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Cascaded Multilevel Inverter Topologies for Photovoltaic Power Generation Systems

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Abstract: The MATLAB based simulation on simulink platform is presented for Single Phase Cascaded symmetric Multilevel Inverter for 5 levels. Theoretical study is done for the classification of multilevel inverter. And also the study is done for the classification of modulation scheme for multilevel inverter. Modulation scheme used for single phase symmetric multilevel inverter is fixed frequency multicarrier pulse width modulation with phase opposite disposition. A comparative study is done for 5, 9, 15, and 25-levels Symmetric Cascaded Multilevel Inverter relevant to harmonics and its harmonic content in Load Voltage and Load Current. The circuit diagram and simulation results with comparative study of total harmonic distortions (THD) are presented.
Keywords: Symmetric cascaded multilevel inverter, PWM, THD.

I. Introduction

In many rural areas continues electricity is not available from grid. The board itself gets power from either hydropower station or thermal power station. As the world's conventional energy source are vanishing fast, with corresponding rise in cost, solar/wind energy offers a good alternative source. It is free, abundant, pollution free and distributed throughout the world. With the present trend of research, the cost of photovoltaic cells is expected to go down in future, making them attractive for wide range of application[4]. Photovoltaic solar energy source have been well known energy source for space application where cost is not consideration, but presently there are number of applications of power solar cells which it needs to be convert to AC power by the use of inverter. Solar cell is providing less output voltage. In order to generate a high voltage source, series connection (array) of cells is required. In a residential photovoltaic system of a few kilowatts in size, the array is mounted on the top of the roof which is the most suitable angle for maximum utilization of the light intensity[5].

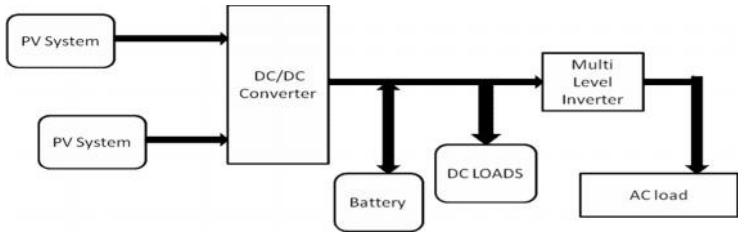

Fig. 1. Photovoltaic Solar Power Generation System

The cascaded multilevel inverter under consideration is capable of minimizing the level of the harmonic contents of the load current waveform. It should not be susceptible to the variation of load and therefore its overall performance is very much superior over the conventional type of inverter. The inverter used here has a configuration of symmetrical cascaded multilevel inverter. The Fig. 1 shows photovoltaic solar power generation system which can use multilevel inverter as one its component that has been presented in this paper.

II. Multilevel Inverter Topologies

Multilevel inverter achieves high voltage switching by means of a series of voltage steps, each of which is depend on the rating of individual power devices. Several topologies for multilevel inverter have been given in the survey[1,2]. They are classified in two groups as shown in Fig. 2, depending on the number of independent DC source. The most famous working topologies are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). The FC and CHB are also known as multi-cell inverter due to its modular structure. An NPC inverter is basically composed of two conventional two-level voltage source inverters stacked one over the other with some minor modifications. The FC topology is some way similar to the NPC, with difference that the clamping diodes are replaced by flying capacitors. CHBs are inverter constructed by series connection of two or more single-phase H-bridge inverters, hence the name is given. A single H-bridge inverter is generating three different voltage levels. CHB provides more redundancies than the previous topologies, since each single H-bridge or modular structure has one redundant switching state; the series connection itself produces more redundancies. Thus redundancy increases as go on increasing power cells for higher levels. These redundancies and the natural modularity of this topology are advantages that enable fault tolerant operation. The main disadvantage of this topology is that each single H-bridge cascaded inverter modules needs a separate DC supply source.

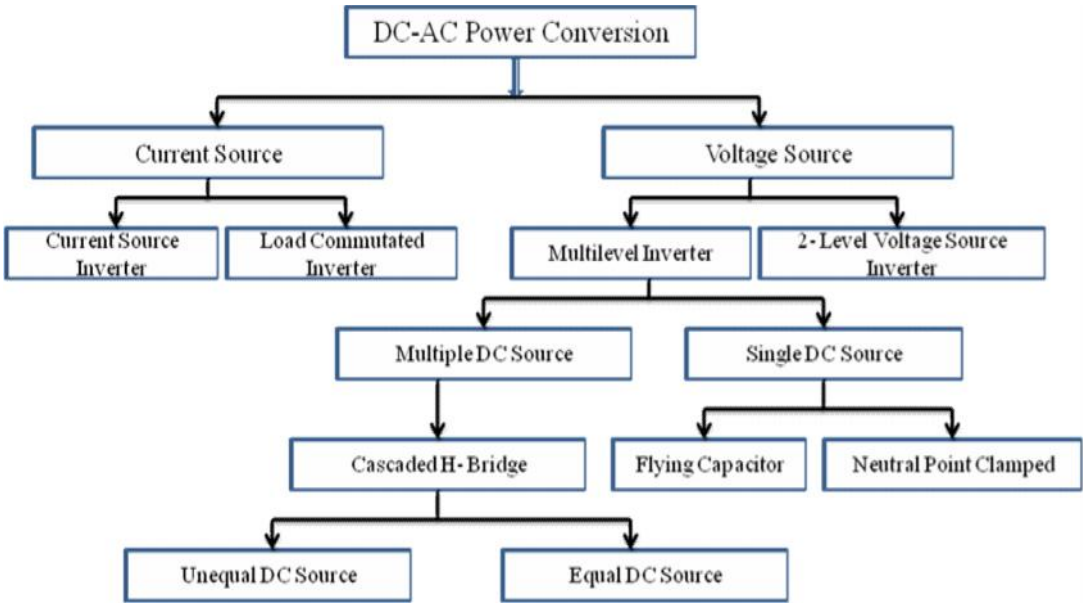

Fig. 2. Classification of Inverter Topologies

This paper is mainly focused on the cascaded multilevel inverter. There are different configurations such as symmetric and asymmetric under the categories of cascaded multilevel inverter which employs equal and unequal DC source respectively. An evaluation of the symmetric cascaded multilevel inverter with different levels has been demonstrated in a detailed manner. A theoretical study and MATLAB simulation of the single phase symmetrical cascaded multilevel inverter with SPWM techniques has been presented. The performance of single phase symmetrical cascaded multilevel inverter employing the above mentioned technique has been evaluated in the term of THD.

A. Symmetric Cascaded Multilevel Inverter

Conventional CHBs are itself called as Symmetric Cascaded Multilevel Inverter (SCMLI). It is formed by the series connection of two or more single-phase H-bridge inverters. Each H-bridge comprises of two voltage

source phase legs, where the line-line voltage is the converter output. Therefore, a single H-bridge (power cell) can generate three different voltage levels. Each leg has two possible switching states, to avoid dc-link capacitor short circuit. Since there are two legs, four different switching states are possible, out these, two outputs are redundant. When two or more H-bridge is connected in series, their outputs can be combined to generate different output levels, increasing the total inverter output voltage and also its rated power. In general terms, when k H-bridges are connected in series, 2k+1 different voltage levels are obtained (two levels per H-bridge and zero level is common to all). The symmetrical cascaded multilevel inverter which is used here consists of two H-bridge which generates output voltage of five levels. Two H-Bridge H_1 and H_2 consists of a separate DC source V_{dc} as shown in Fig.3. Let the output of H_1 be denoted as $V_{o1}(t)$, the output of H_2 be denoted as $V_{o2}(t)$. Hence the total output voltage is given by $V(t) = V_{o1}(t) + V_{o2}(t)$. By alternately opening and closing the switches S1, S4 and S2, S3 of H_1 appropriately, output of H1 V1(t) can be made equal to +Vdc, 0 or -Vdc. Similarly other H-bridge gives output voltage +Vdc, 0 or -Vdc. Hence V(t) takes values $2V_{dc}$, -Vdc, 0, +Vdc, +2Vdc, as shown in the Fig. 3.

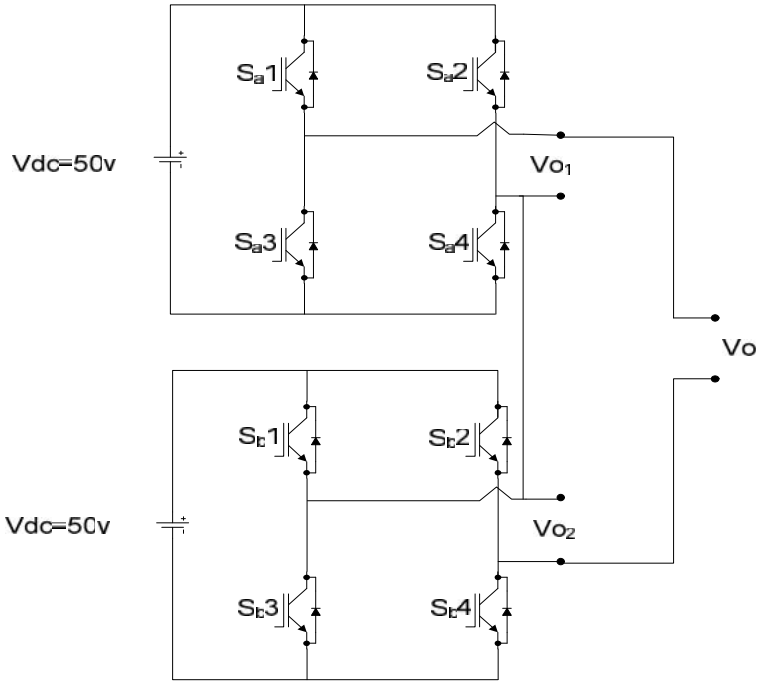

Fig. 3. Symmetric Cascaded Multilevel Inverter

III. Modulation And Control

There are many modulation techniques employed for multilevel inverter[3,4]. Fig. 4 shows the multilevel inverter modulation methods. Selective harmonic elimination (SHE) is one the modulation technique for low switching frequency which used in very high-power application. Among them multicarrier PWM techniques is extensively used. Multicarrier PWM technique is characterized in four categories, as shown in Fig. 4.

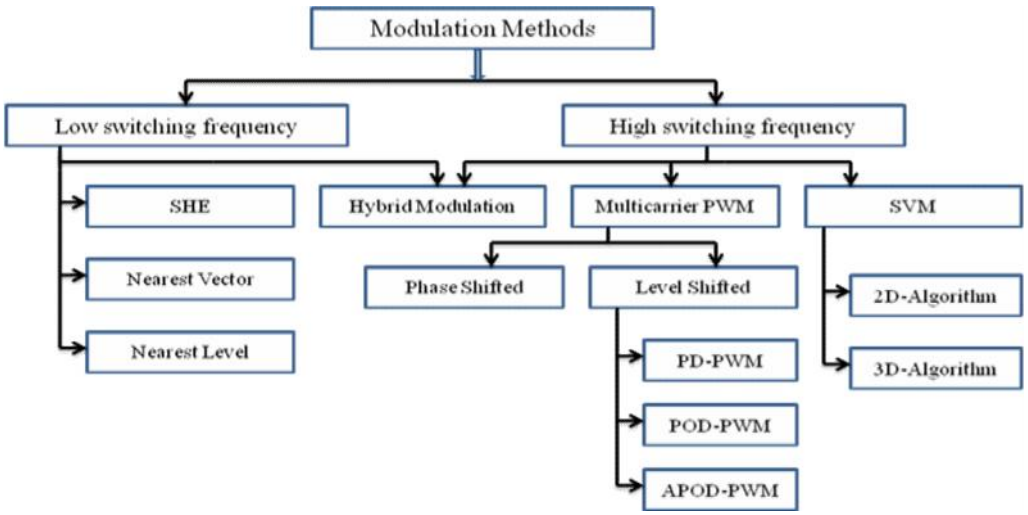

Fig. 4. Classification of Modulation Methods

A. Fixed Frequency PWM Technique for symmetrical Cascaded Multilevel Inverter

It is generally seen that the performance of any inverter, with any switching scheme can be related with the harmonic contents in its output voltage. Phase opposition disposition (POD) is used in this paper; it has less harmonic distortion on the line voltage. It uses the same reference sinusoidal signal as the conventional SPWM while the carrier signal which is triangular one is a modified one. To implement an m-level inverter, (m-1) carriers are used. There are four distinct carriers with fixed frequency and with the same magnitudes; the difference between the carriers is that they are all displaced by a set of DC offset. The carrier signals from C1 to C4 have same frequency. The pulses will generate when the amplitude of the modulating signal will be greater than that of the carrier signal. The number of switching per modulation cycle (t) in each level of the inverter is dependent on the carrier frequency for that level and the duration of time that the reference waveform dwells within the level's corresponding time band. If the carrier frequency for all the levels is identical, the top and bottom levels will have more switching than the intermediate levels. In order to balance the switching action, the carrier frequency of each band is varied (known as Variable Frequency PWM) based on the time duration that the reference waveform dwells in the carrier band. In cascade multilevel inverter, the four gate pulses for the two H-bridge are generated by comparing the reference signal with the four carrier signals, as shown in fig. 5. The reference signal is taken as sinusoidal and the carrier signals C_1, C_2, C_3, and C_4 as triangular. The carrier signals are compared with the reference signal using a comparator and four output signals are produced. These signals are given as input to logic gate to produce eight output signals. This signal is given to the eight switches of the two H-bridge to produce a five level output waveform. The switching scheme for 5-level SCMLI is given in Fig. 6.

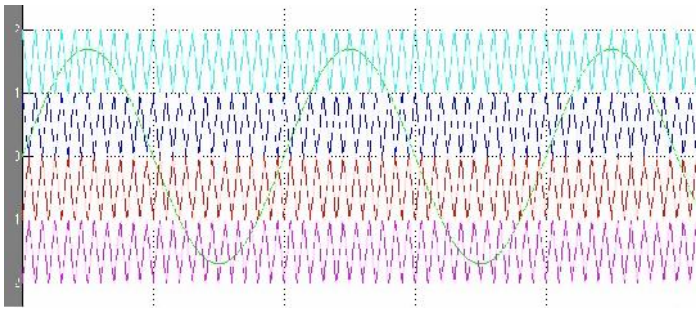

Fig.5. Gate Pulse for SCMLI

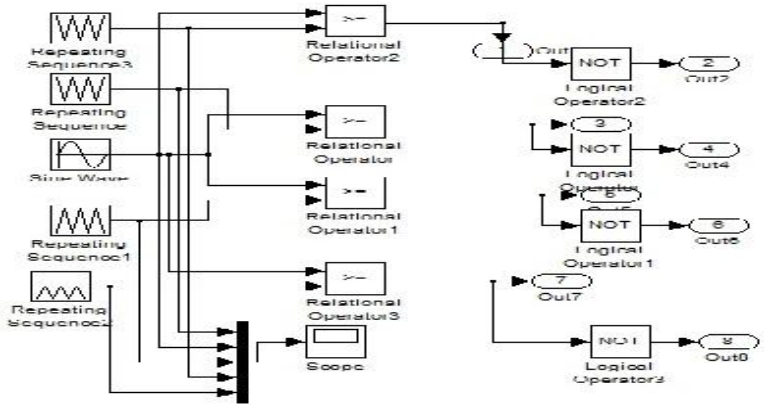

Fig. 6. Switching scheme for 5-level SCMLI

IV. Simulation Results

Symmetric Cascaded Multilevel inverter with 5-level is simulated using MATLAB-Simulink. Here load is taken as RL load, output voltage and load current characteristics are shown in Fig. 7 and Fig. 8.

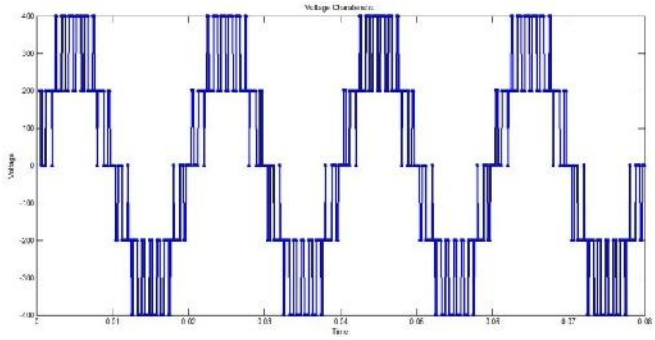

Fig. 7. Voltage Characteristic

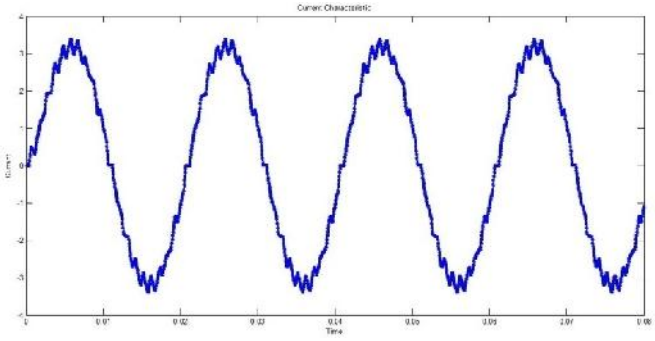

Fig. 8. Current Characteristics

A. Comparative study of Harmonic analysis for SCMLI

This paper has presented Total Harmonic Distortion (THD) analysis for Symmetric Cascaded Multilevel Inverter (SCMLI). Here comparative study is done from 5^{th} level to 25^{th} level for output voltage and load current. The harmonic contents are analyzed up to 7^{th} harmonics in various levels of outputs are shown in Table 1 and Table 2 respectively.

Table 1: Harmonics in output voltage for various level of SCMLI

Serial No.	Number of Level	THD (%)	Harmonic Contents (%)		
			3^{rd}	5^{th}	7^{th}
1	5	37.72	1.13	0.20	0.02
2	9	14.83	2.32	0.18	0.45
3	15	9.32	1.27	2.37	2.07
4	25	5.33	0.11	0.44	0.60

Table 2: Harmonics in load current for various level of SCMLI

Serial No.	Number of Level	THD (%)	Harmonic Contents (%)		
			3^{rd}	5^{th}	7^{th}
1	5	5.39	0.86	0.11	0.01
2	9	3.85	2.05	0.13	0.28
3	15	2.13	0.97	1.33	0.46
4	25	0.78	0.09	0.25	0.26

The THD of output voltage and load current for a 25-level SCMLI has been shown below in Fig. 9 and Fig.10 respectively.

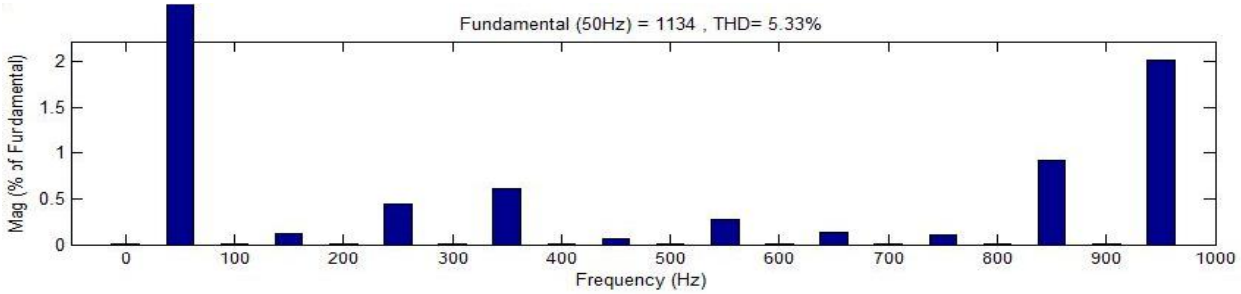

Fig. 9. THD analysis of output voltage for 25-level SCMLI

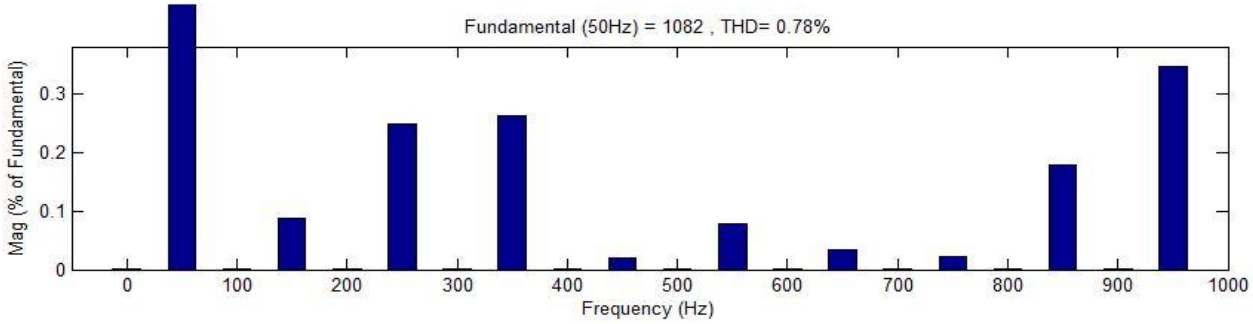

Fig. 10. THD analysis of load current for 25-level SCMLI

V. Conclusion

The Cascaded Multilevel Inverter is Suitable for PV Solar power generation .It has a possibility of generation of Stepwise nearly sinusoidal output load voltage with Minimum Harmonics. Therefore filter requirement is eliminated. Presented circuit is providing separate DC supply for each module, which is a good option for photovoltaic solar power generation system. It is easy to build and it has more redundancy than any other topologies. Presented topology has high efficiency. If this inverter is used in rural areas for photovoltaic systems, than this Multilevel inverter will be a good alternative to grid supply in rural industries.

Abbreviation

THD- Total Harmonic Distortions.
PV System- Photovoltaic System
NPC- Neutral Point Clamped
FC- Flying Capacitor
CHB- Cascaded H-bridge
SPWM- Sinusoidal Pulse Width Modulation
SCMLI- Symmetric Cascaded Multilevel Inverter
SHE- Selective Harmonic Elimination
POD- Phase Opposition Disposition

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