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A Compact SPICE Model for Asymmetric Drain Spacer Extension FinFET

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Abstract: Multi-gate devices like FinFETs can be used in the nanometer regime to reduce short channel effects encountered by planar MOSFETs. Along with the scaling advantages, FinFETs face the problem of width quantization**.** To overcome this, an advanced architecture, Asymmetric Drain Spacer Extension (ADSE) FinFET was proposed. This is a comparatively new device and the modeling and applicability analysis is still in its infancy. Till now no compact SPICE model is proposed for this device which helps circuit designers to analyze its performance at circuit level. This paper is trying to fill that literature gap. In this paper, a new compact SPICE model is proposed for ADSE FinFET. The model was verified against the published results in the literature. Obtained simulation results agreed with the published results from analytical models. This model was later used for the performance analysis of the device at circuit level. This is followed by a comparison of its performance against planar devices at the circuit level. This was done by evaluating the performance of ring oscillator circuit. This was done for a fixed underlap length. The major observations from this analysis are: FinFET is better than MOSFET in terms of drain current and frequency response and the power dissipation of underlap device is less than that of corresponding device with no underlap. The propagation delay of underlap device is less than that of normal device.

1. Introduction

The advancement of CMOS technology is primarily due to scaling. However, as devices shrink to the nanometer regime, the subthreshold leakage current of planar MOSFETs drastically increase. This is the result of the drain competing with the gate to get control over the channel. To counter this, at gate lengths below 50nm, the channel should be controlled from more than one side[1].

In this context, multiple-gate field-effect transistors (MGFETs) emerged as an alternative. They exhibit better screening of the drain potential from the channel due to the presence of additional gates close to the channel. Among all MGFETs, FinFETs have emerged as the most desirable substitutes to MOSFETs due to their simple structures and ease of fabrication. In this device, the gate wraps around the channel as given in Fig.1. This helps in increasing the gate control resulting in further reduction of the gate length. In the figure, the gate length of the FinFET is L_G, fin height is H_{fin} and the fin width is T_{si}.

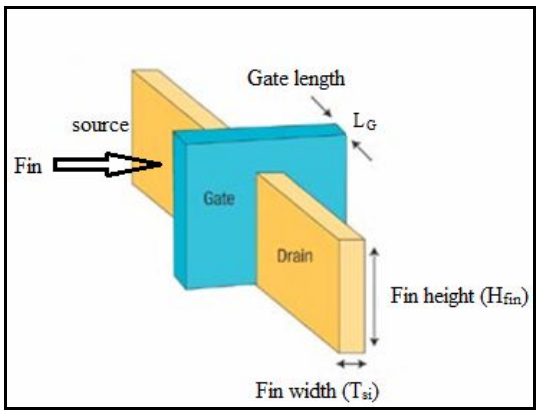

Fig. 1 Structure of FinFET

FinFETs have a vertical channel (fin) compared to the horizontal channel of planar MOSFETs. This means that, the fin height (H_{fin}) determines the channel width (W) for FinFETs. This sets a limitation on the width of the channel length. i.e., width can increase only in multiples of silicon fin height. This is known as the 'width quantization problem' and is a major drawback for FinFETs. Due to this, FinFETs cannot be used for designing circuits where transistor sizing is important [e.g., flip-flops, pseudo (NMOS) logic etc.] [2].

ADSE FinFET or Asymmetric Drain Spacer Extension FinFET was introduced to tackle this problem. What makes this device different from ordinary FinFET is its drain side underlap. Although, the ADSE FinFET structure has been proposed, to the best of our knowledge, there is no existing SPICE model to analyze the effect of ADSE structure. This paper aims to fill that literature gap by proposing a compact SPICE model for ADSE FinFET. Using the proposed model, device performance comparison is done at the circuit level.

The SPICE model for a double gate device like FinFET can be developed from that of a single gate device. Similarly, SPICE model for ADSE FinFET can be obtained from that of a single gate device with only drain side underlap. Such a single gate device is the ASDE MOSFET or Asymmetric Source/Drain Extension MOSFET[3]. The idea of developing the SPICE model of this MOSFET is extended to develop the model for ADSE FinFET.

The rest of the paper is organized as follows**:** In section 2, a review of literature is given. Section 3 deals with the equivalent circuit model for ADSE FinFET. In section 4, circuit level performance using ring oscillator circuit is evaluated and finally section 5 concludes the paper.

2. Review of Literature

As said earlier, highly scaled MOSFETs perform poorly as a switch due to increased short channel effects. Considerable research was conducted to find a solution to this problem and one of the promising techniques was the introduction of underlap. Underlap minimizes the gate-to-source/drain overlap capacitance which, in turn, reduces the switching power and the circuit delay. Underlap can be introduced on both source and drain sides. However, underlap on the source side degrades the saturation current due to high resistance of the source. So, only drain side underlap is preferred. This technique can be applied to MOSFETs and FinFETs. MOSFETs with drain side underlap is the Asymmetric Source/Drain Extension MOSFET. The device and its SPICE model has been reported in[3]. Similarly, Asymmetric Drain Spacer Extension FinFET has been introduced in[2]. In this section, we review the state of art in research in the case of both device architectures such as ASDE MOSFET and ADSE FinFET.

2.1. ASDE MOSFET

In ASDE MOSFET, underlap has been provided only at drain side. In addition to the advantages of reduced power and delay, as the drain moves away from the channel, the short channel effect due to drain induced barrier lowering (DIBL) improves considerably. While it has the disadvantage of poor ON state device drive current due to rise in channel resistance. Therefore, there exists an optimal gate-to-source/drain underlap length for a particular device in terms of circuit performance. A detailed study of the effect of underlap in MOSFETs has been given in[3].

2.2. ADSE FinFET

ADSE FinFET structure was introduced to overcome the 'width quantization problem' .Different underlap lengths result in different drain currents and thus the width quantization problem is solved. ADSE FinFETs also exhibit improved Short Channel Effects due to an indirect increase in channel length. On the other hand, underlap calls for increased layout area. Moreover, asymmetry in underlap results in asymmetry in current which means that source and drain are not interchangeable. This affects the performance of the device as pass transistor[3].

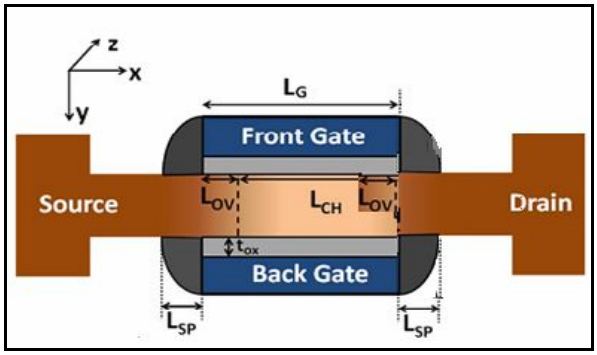

Fig 2: Structure of normal FinFET

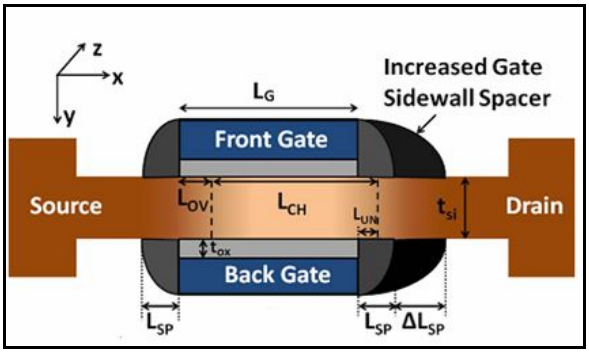

Fig 3: Structure of ADSE FinFET

Fig 2 shows the structure of a normal FinFET and Fig 3 shows that of ADSE FinFET. In the figures, L_G represents the gate length and L_{CH} is the channel length. t_{ox} is the oxide thickness and t_{si} represents the fin thickness. L_{ov} is the gate to source/drain overlap length. In ADSE FinFET, drain side underlap (L_{UN}) is made possible by introducing an additional offset spacer only on the drain side i.e., the nominal sidewall spacer thickness (L_{SP}) is increased by ΔL_{SP} to introduce gate underlap on the drain side. On the source side, gate–source overlap (L_{OV}) exists as in conventional FinFETs. But, the gate length (L_G) is not changed[2].

3. Equivalent circuit model for ADSE FinFET

In this section, we deal with design and simulation. Analytical models were developed first using the MATLAB tool and later these models were incorporated into the SPICE compatible transistor model. The proposed model is discussed in section 3.1 and its validation methodology in 3.2.

3.1. Circuit Level Model

This work was carried out under a limited focus to develop a model for the analysis of switching characteristics. The technology node under consideration throughout the work is 32 nm. The underlap length for the drain side is fixed as 2nm for the SPICE model verification. The SPICE model for ASDE MOSFET was discussed in literature[3].This is revised to form the SPICE model for the analysis of switching characteristics. The revised model is given in Fig.4. The basic idea used for the development of this model is from the equivalent circuit model of a BSIM 4 PDSOI transistor. In this model, R_d and R_s represent the drain and source resistances respectively, C_{gs} is the gate to source capacitance and gm is the transconductance. These are same as that of normal MOSFETs. V_{gs} represents the gate to source voltage and V_{ds} represents the drain to source voltage. In order to model the reduction of drain current due to the reduction of drain overlap extension in

ASDE transistors, one current controlled current source (CCCS), M_4 is added. This goes from the source to the drain and the value of current for M_4 depends on the drain current of the reference device (without ADE reduction). The gain of this CCCS (α) is chosen based on the analytical models developed using MATLAB tool. In addition, the impact of drain underlap on the drain-to-gate capacitance (C_{gd}) is modeled by changing the existing BSIM4 parameters. The revisions for underlap are highlighted in Fig 4.

The revised model includes one additional Current Controlled Current Source and revised capacitance parameters affected by underlap.

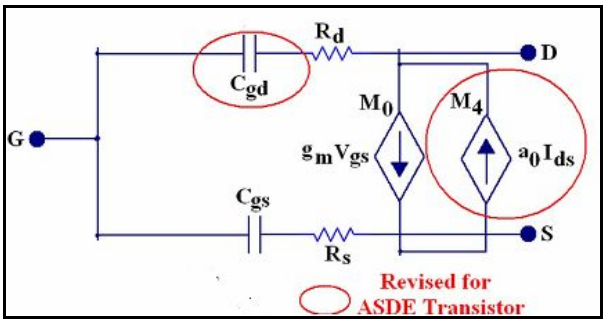

Fig 4: Transistor model for ASDE MOSFET considering only the switching characteristics

The values for C_{gs}, R_d, R_s, $I_{d(ref)}$ and g_m were calculated from BSIM equations using MATLAB tool[4]. The values are: C_{gs}= 0.14nF, R_d= 138.8Kand R_s= 138.8K. These values were then used in SPICE model.

3.1.1 Development of the model

The reference ADSE FinFET device, whose model was developed has the specifications as in table 1:

Table 1: Specifications for the proposed model

Parameter	Value
Physical gate length (L_G)	32 nm
Oxide thickness (Tox)	1.6nm
Thickness of gate (Tpoly)	60nm
Silicon body thickness (Tsi) (fin thickness)	9nm
Fin height (Hfin)	44nm
Fin Pitch (P)=Fin Width	22nm
Body doping	intrinsic
Source/Drain Doping	1e20 cm^{-3}
Overlap Length for gate and Source (Lov)	3.5nm

At first, two single gate ASDE MOSFETs were cascaded in a parallel fashion to get the ADSE FinFET model. The arrangement is shown in Fig.5**.**

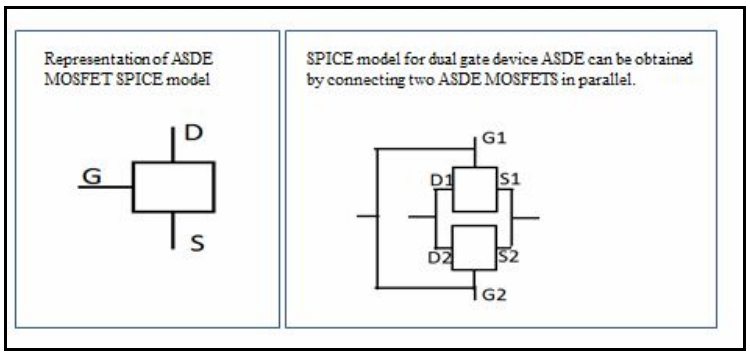

Fig. 5: Development of ADSE FinFET from ASDE MOSFET

The simulation results with the above model showed a significant difference from the published results [2]**.** This suggested that a fitting parameter is required for the FinFET. This fitting parameter should be related to fin height and pitch which represent the third dimension of a FinFET. A well-established relationship between the current drive of a multigate FET and that of a single gate, planar MOSFET has already been described in [5]**.**For this, they should have the same gate area**.** This relationship is given in equation (1).

Considering a pitch P for the fins, the current in the multigate device (I_D) is given by,

$$I_D = I_{D0}\frac{\theta\,\mu_{side}W_{si}+2\mu_{side}.t_{si}}{\mu_{top}.P} \qquad (1)$$

Where I_{D0} is the current in the single gate, planar device, W_{si} is the width of each individual fin, t_{si} is the silicon film thickness, and θ = 0 in a FinFET where channels are formed at the side wall interfaces only. μ_{side} is the side wall mobility and μ_{top} is the topside mobility [5].

By applying the values for FinFET in equation (1), the drain current will be as in equation (2):

$$I_D = 2.I_{D0}.\frac{\mu_{side}}{\mu_{top}}.\frac{t_{si}}{P} \qquad (2)$$

From this we can deduce the value for the fitting parameter (f_p) required to convert a planar ASDE MOSFET to ADSE FinFET. This is given in equation (3).

$$f_p = 2.\frac{\mu_{side}}{\mu_{top}}.\frac{t_{si}}{P} \qquad (3)$$

When we cascade two ASDE MOSFETs, (f_p) will be reduced by half. The new value α will be as in equation (4):

$$\alpha = \frac{\mu_{side}}{\mu_{top}}.\frac{t_{si}}{P} \qquad (4)$$

The drain current equation after the introduction of α will be:

$$I_D = I_{D0}.\alpha \qquad (5)$$

The reference FinFET has only a single fin. So Pitch is the same as fin width. t_{si} is 2 times P.[5] . Here we also assume $\mu_{side} = \mu_{top}$. Then, I_D will be as in equation (6).

$$I_D = 4.I_{D0} \qquad (6)$$

The final proposed model is developed by incorporating the parameter (α) in the model in Fig.5. The SPICE model for ADSE FinFET with only the switching characteristics is given in Fig.6. In addition to the parameters for the ASDE MOSFET, the gain of CCCS gets multiplied by the factor α.

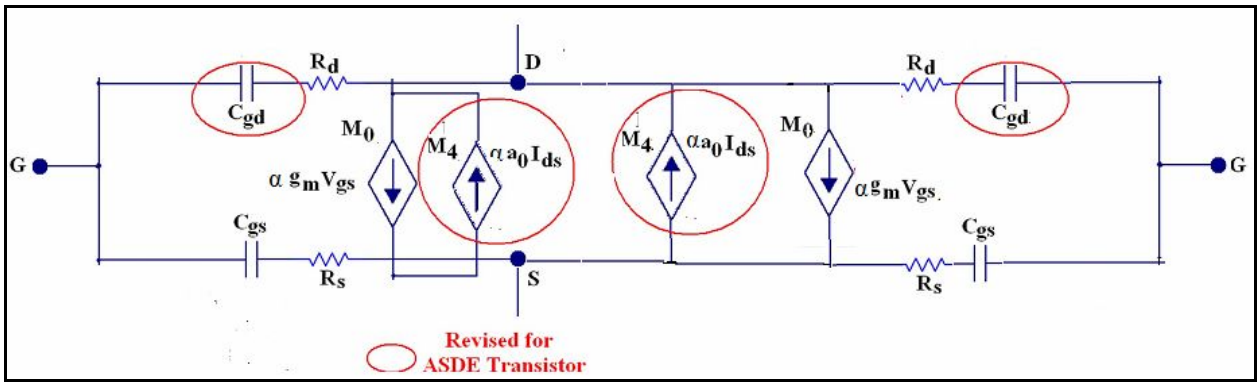

Fig 6: Proposed SPICE model for ADSE FinFET

Where $\alpha = \frac{\mu_{side}}{\mu_{top}}.\frac{t_{si}}{P}$

3.2 Validation of the model

The first step was analytical modelling and for this, ASDE MOSFET underlap length was varied from 0 to 4nm. Corresponding to this, the side wall spacer length varied from 3.5nm to 7.5 nm[6]. The graphical representation of the results are given in Fig.7.

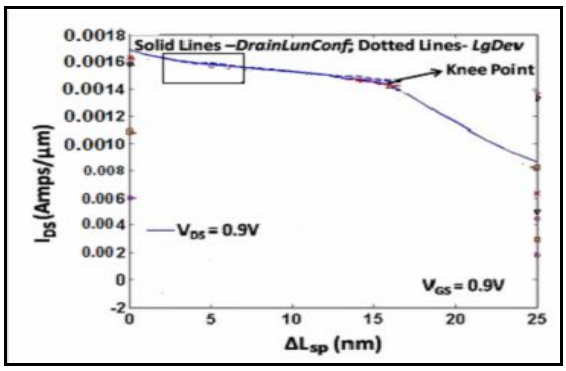

Fig 7(a): Drain current for ADSE FinFET for different ΔLsp (published result (2))

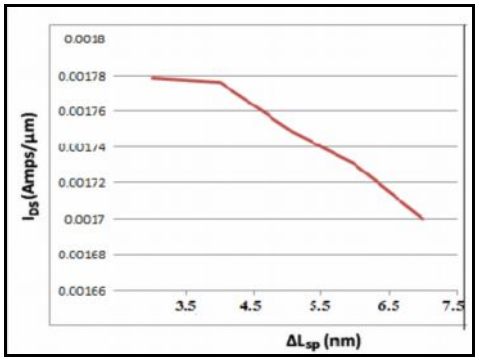

Figure 7(b): Drain current for ADSE FinFET for different ΔLsp(simulated result)

In the published work,[2] , it can be seen that the drain current ranges between 1.66e-03 A/µm and 1.62e-03 A/µm for ΔL_{sp} ranging from 3.5 to 7.5 nm (approximate values). The simulated result ranges between 1.778e-03 A/µm and 1.7e-03 A/µm. This indicates that the results obtained in this paper almost agree with the results that have already been published.[2]

After the validation of the analytical models, the derived values were used in the SPICE model development.

4. Circuit level performance evaluation

Circuit level performance analysis was done using ring oscillator circuits. Propagation delay and power dissipation were the parameters that we tried to analyze using the proposed model.

Ring oscillator circuits are often used as prototype circuits to test new semiconductor processes. This is a circuit composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing *true* and *false*. The frequency of oscillation is given in equation (7) as:

$$f_o = \frac{1}{2m\tau_d} \qquad (7)$$

where m is the no: of delay stages. Thus the propagation delay of an inverter circuit can be obtained by measuring the time period of the oscillator. In this paper, simulations were done with a 31 stage ring oscillator and the circuit is given in Fig. 8.

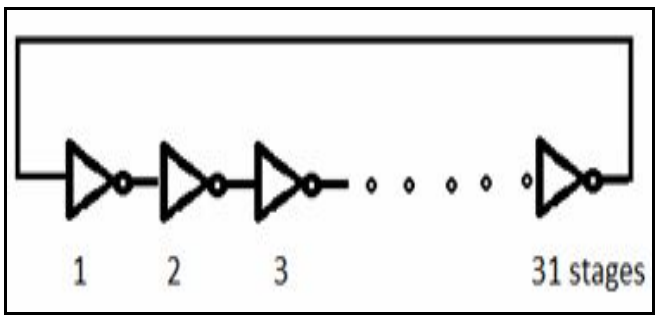

Fig.8: A 31stage ring oscillator

The inverter circuit was designed using NMOS devices with enhancement load assuming W=L for the active device. The inverter circuit used is given in Fig.9.

Ring oscillators with planar MOSFET, ASDE MOSFET, normal FinFET and ADSE FinFET were simulated for the performance comparison.

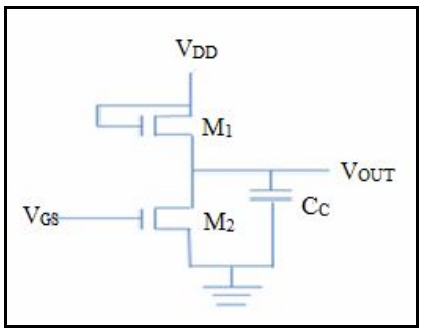

Fig. 9: Basic building block for ring oscillator

4.1 Performance analysis of Ring Oscillator using planar MOSFET and ASDE MOSFET

Fig. 10 shows ring oscillator output waveform for MOSFETs. In Fig. 10, we can see that the frequency of normal MOSFET is 17.5MHz while that of ASDE MOSFET is 7.1 MHz .

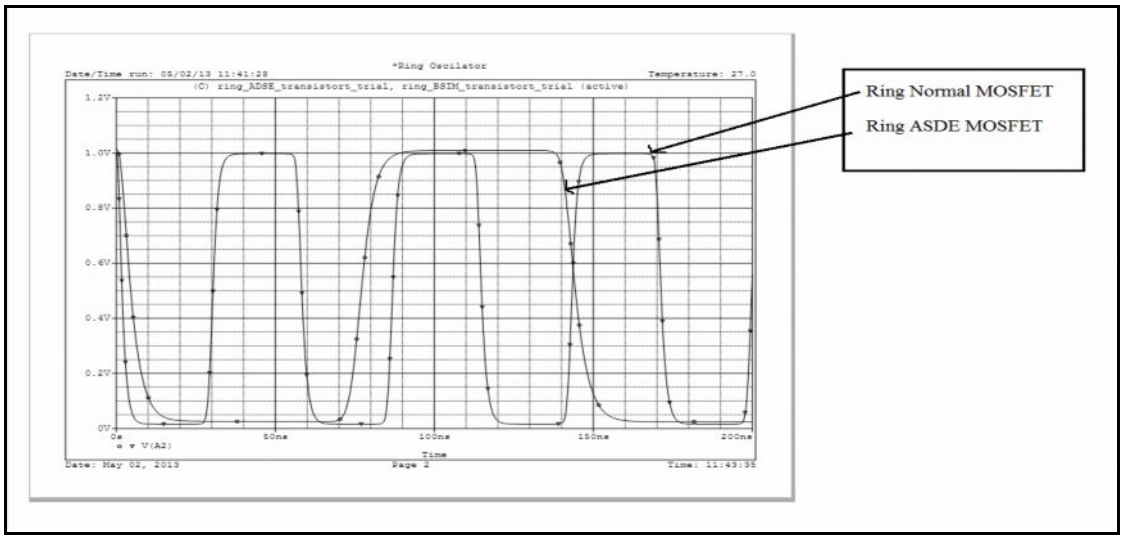

Fig.10: Ring Oscillator output waveform using MOSFETs

4.2 Performance analysis of Ring Oscillator using Normal FinFET and ADSE FinFET

Fig. 11 shows Ring Oscillator output waveform for FinFETs. In this, the normal FinFET has a frequency of 17.7GHz while ADSE FinFET has a frequency of only 7.2GHz.

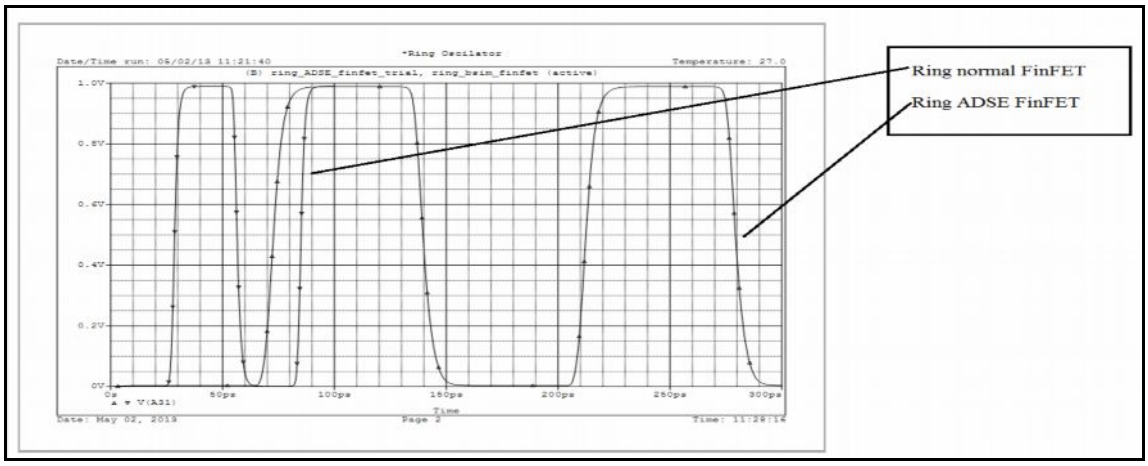

Fig. 11: Ring Oscillator output waveform using FinFETs

4.3 Comparison of ring oscillator performance of ADSE FinFET with other devices

Table 2 gives a comparison of Ring Oscillator circuit performance of different devices. The underlap length is 2nm.

Table 2 : Comparison Table for Ring Oscillator

Parameter	Mosfet		Finfet		Remarks
	NORMAL	ASDE	NORMAL	ADSE	
Time period	57ns	140ns	56.5ps	140ps	
Frequency	17.5MHz	7.1MHz	17.7GHz	7.2GHz	Frequency of FinFET greater than that of MOSFET
Propagation delay	1.84ns	4.52ns	1.823ps	4.52ps	For 2nm,underlap leads to greater propagation delay
Power Dissipation (W)	0.146	0.0591	0.291	0.118	For 2nm,underlap leads to less power dissipation

The following inferences can be made from the table: 1. FinFET is better than MOSFET in terms of frequency and 2. Power dissipation of underlap devices (for 2nm) is less than that of corresponding devices with no underlap. 3. Also, the propagation delay of underlap device is greater than that of normal device. There is an optimal underlap length for optimum circuit power delay product (PDP) [3].

5. Discussion

In this paper, a compact SPICE model is proposed for ADSE FinFET. Using this model, performance comparison using ring oscillator circuit is done. There are some limitations for this work: The focus of the work was limited to develop a model for the analysis of switching characteristics. This was done for a fixed drain underlap length. Also, only NMOS devices could be considered. If the underlap length is varied, there will be an optimal underlap length for optimum circuit power delay product (PDP) .These factors can be considered for extending the work in future. It is expected that the proposed SPICE model will facilitate circuit designers to evaluate the relative advantages of using these devices in various applications.

6. References

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