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Design of FinFET Based LNA with reduction of Corner Effects

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Abstract: The influence of the corner effects on the FinFET that is designed with 30nm gate length technology is investigated. Heavy doping at the corners is employed and its effect on ON-current is studied. A mixed mode device, low noise amplifier is to be constructed with the modeled FinFET and using Source Degeneration Inductor. Noise figure and gain which are key parameters for the LNA are studied by varying the geometric parameters of the device. Also, the metals for the contacts which induce delay in the circuit are replaced with vias. The gain and noise figure of the high frequency LNA is studied using the Silvaco TCAD and Sentarus TCAD simulations from Synopsys.
Keywords: FinFET, LNA, , Noise Figure.

Introduction:

Scaling limitations of conventional bulk MOSFETs demand the need for novel devices. Many novel device structures have evolved to overcome the scaling limitations of conventional bulk MOSFETs. FinFETs are predicted as one of the best possible candidates to replace the bulk MOSFETs in the sub45-nm regime due to their improved subthreshold slope, reduced leakage current, better short-channel performance, and compatible process flow with existing CMOS technologies. FinFET, a novel double-gate structure, in which the Silicon fin forms the channel and gate wraps around the fin. Silicon fin has insulator on top and gate on either side, current flows parallel to the device surface.

Scaling of the conventional bulk Si MOSFETs have slowed down,due to short channel effects (SCE) coming into picture such as V T roll-off, hot carrier effects, drain induced barrier lowering (DIBL),increase in subthreshold swing and leakage currents, etc. So, to avoid short channel effects we require performance boosters, like use of novel materials and non-classical device structures to continue further scaling. These replacable candidates are multi-gate MOSFETs called FinFETs. As the gate length decreases the gate control over the channel also decrease due to the proximity of source and drain. The gate control over the channel can be improved by geometrically placing the gate close to the channel and providing tighter gate coupling. The gate can be placed close to the channel by taking ultra thin body known as fin type structure and tighter gate coupling can be achieved by increasing the number of gates from single gate to multi gate. The multi gate FinFET transistors are very promising alternatives to planar devices in sub 45nm gate length regime. To facilitate this, a device generated with reduction of corner effects which leads to increase in output and improved sub threshold slope[1-7].

[1-7]Communication technology is always moving to higher frequency bands. To facilitate this, the devices used in the RF transceiver are shrinking in size. A low noise amplifier (LNA) is a critical block in RF transceivers.LNA is a key component in RF front-end receivers which poses a major challenge in terms of meeting high gain and low noise figure at low power supply voltages. In this work, a FinFET-based LNA is designed and simulated in TCAD simulator, and analyzed for the impact of various geometrical parameters on LNA performance. Simulations are performed at 2D level. At 2D level, we have the opportunity to change six different geometrical parameters, gate length(Lg), fin width (Wfin), gate oxide thickness (Tox), source/ drain underlap (Lun), source/drain width (SW), and source/drain length (SL) of the device. As LNA uses two transistors, there are twelve parameters to vary. The above parameters are varied to capture their sensitivity on LNA parameters such as input impedance (Zin), gain (S21) and noise figure (NF). Next section deals with the simulation methodology and extraction procedure of LNA parameters from the simulation results. Simulation results are discussed in section III. Finally, section IV gives the conclusion.

Simulation Methodology And Extraction[1-7].

Simulation Methodology

Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations
- Inspect and Tecplot: To view the results.

Mixed mode simulation facility of SDEVICE is used to investigate the performance of LNA. The physics section of SDEVICE includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. Noise models such as diffusion noise, monopolar generation-recombination noise, bulk flicker noise are included while doing noise simulations. The 2-D structure generated using SDE is shown in Fig. 1. The 3-D structure generated using SDE is shown in Fig. 2.Fig.3 shows the schematic diagram of the device. The various parameters of the device can be seen in Fig.3.

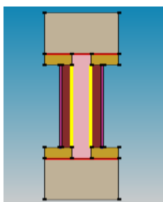


Figure 1: Structure generated from TCAD

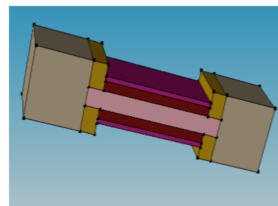


Figure 2: Structure of 3D FinFET

Schematic view of 2D FinFET:

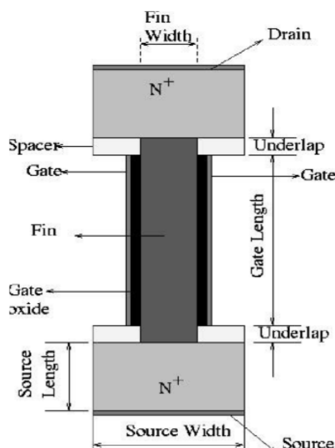
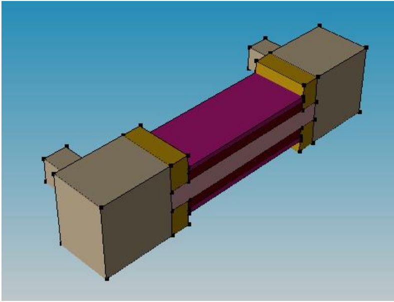


Figure 3.Schematic view of Dual-Gate FinFET

3-D FinFET with vias:



Here the vias are used to reduce the inter connect delays between the devices at the time of mixed mode simulations. These vias are made up of metals. Here the vias are usually of length 10nm.

Procedure for reduction of corner effects:

The modeled FinFET is containing some corner effects which tends to leakage of electrons and causes hot carrier effects,and fringing field effects. Hot carrier effect: It causes when the electrons escapes from the channel towards the gate terminal.

Fringing field effect: Electric field lines which are from source to channel and drain to channel can take round near to the centre of the channel but not at the corners of the channel and moves away from the channel which causes fluctuations in the output drain current.To reduce this phenomenon we introduce heavy doping at the corners with both n-type or p-type materials.

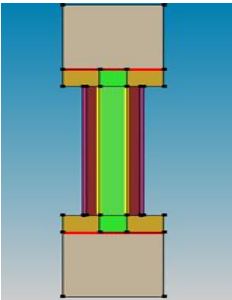


Figure.5: 2-D FinFET with doping

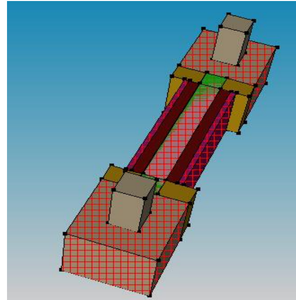


Figure.6:3-D FinFET having vias with doping at corners

Extraction Procedure of LNA parameters

The LNA circuit used in this study is shown in Fig. 3. Generally, a common source LNA is used with a source degeneration inductor to get the impedance match, especially to get the real part of input impedance. But, this circuit does not use any source inductor. Instead, it exploits the non-quasi-static (NQS) effects or the channel resistance which arises due to finite charging time of the channel carriers to get impedance match[2]. An input impedance of 50 Ω, purely resistive, is desired for LNA. The imaginary part i.e. the capacitive part of the input impedance is canceled at the given frequency, by connecting an appropriate inductor at the gate (Lg). This impedance match is done only for the nominal values of the device parameters. SDEVICE simulator is used for mixed mode simulation of LNA circuit (Fig. 3). Transistors T1 and T2 are simulated at the device level. Other elements are simulated using the compact models at the circuit level. Inductors, LG and Lo are used with their series resistance incorporated, and a quality factor of 5 is assumed. Resistances associated with the inductors are given by,

$$R = \frac{2\,\pi\,\text{f.induc or value}}{\text{quality}} \qquad (1)$$

The circuit is operated at the supply voltage of Vdd = 1 V, Vgs of T1 = 0.5 V and Lo = 1.5nH. The operating frequency of LNA is taken as 10 GHz.

Circuit diagram of proposed LNA:

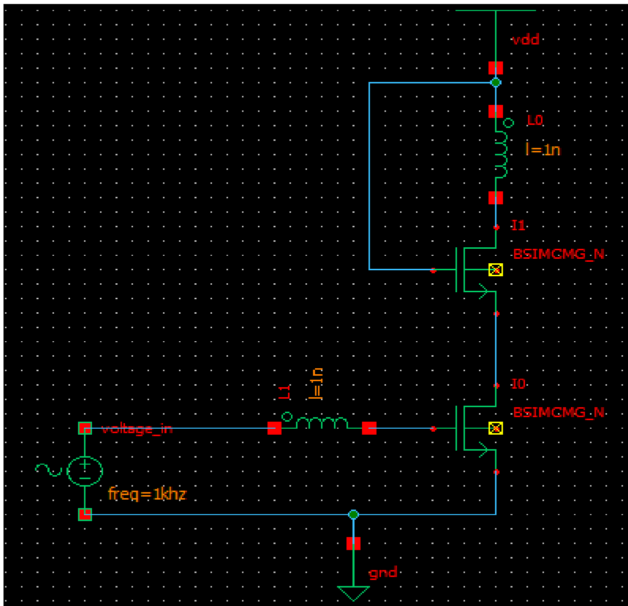


Figure:7. Proposed circuit for LNA

The standard AC simulations are done over a range of frequencies. SDEVICE outputs are in the form of admittance and capacitance matrices. They are converted to S parameter and S21 is taken as gain of LNA. From SDEVICE outputs, Zin is calculated. Noise simulation in SDEVICE is standard AC simulation with noise models included in the physics section. Noise-figure (NF) calculation is done by assuming a signal source resistance (purely resistive) of 50 Ω.

For or a two port network NF is defined as [3,4]

$$NF = 1+\frac{1}{S_I^S}\{S_I^{gg}+|\alpha|^2 S_I^{dd}\text{-}2\mathrm{Re}(\alpha S_I^{dg})\} \qquad (2)$$

with

$$\alpha = \frac{Y_s + Y_{11}}{Y_{21}} \qquad (3)$$

where SIS is the current noise spectrum of the noisy source admittance and is given by,

SIS = 4kBTRe (YS) (4)

are the current noise spectrums, at the gate and drain terminals respectively, is the cross-correlation noise spectrum between the drain and gate terminals, Y11 and Y21 are the respective admittance (Y) parameters.

Six different geometrical parameters, gate length (Lg), fin width (Wfin), gate oxide thickness (Tox), source/drain underlap (Lun), source/drain width (SW), and source/drain length (SL), related to both the FinFETs in the LNA circuit are varied to capture their sensitivity on LNA parameters. So totally there are twelve parameters considered in this study. Table I gives the dimensions of the nominal device and Table II gives the range for the various parameters studied in this paper. Throughout the study channel doping are maintained at 1x1018/cm3.

Table I. Typical device dimensions

Parameters	Nominal Value
Gate Length	30 nm
Fin Width	4 nm
Source width	15 nm
Source length	15 nm
Gate oxide thickness	2 nm
Underlap	4 nm
Channel depth	12nm

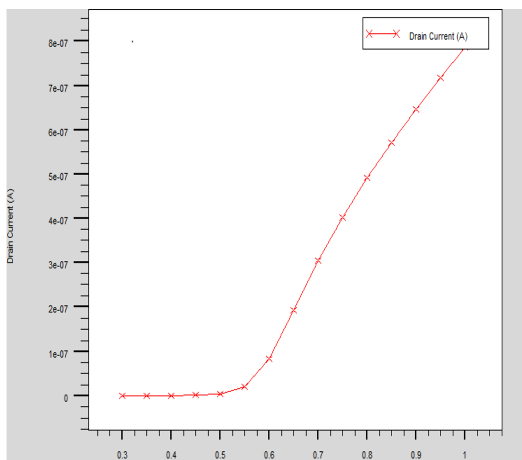
Table II Range of various parameters

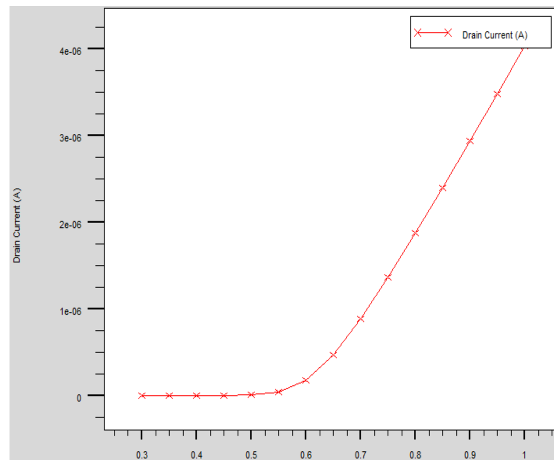
Parameters	Range
Gate Length (Lg1 and Lg2)	20 nm to 40 nm
Channel depth (Ld)	10nm to 15nm
Fin Width (Wfin1and Wfin2)	2 nm to 9 nm
Source width (SW1 and SW2)	10 nm to 20 nm
Source length (SL1 and SL2)	10 nm to 20 nm
Gate oxide thickness (Tox1 and Tox2)	1 nm to 3 nm
Underlap (Lun1 and Lun2)	1nm to 10 nm

Results and discussion

Gate Voltage versus drain current:

The graphs shown below are between input gate voltage and drain current with and without the corner effects.





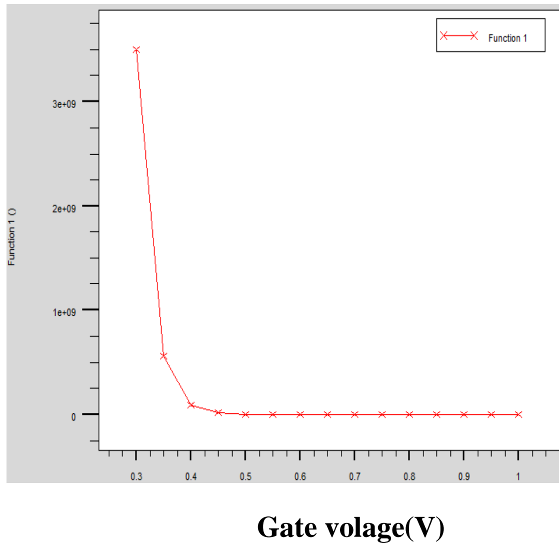
Gate volage(V) **Gate volage(V)**

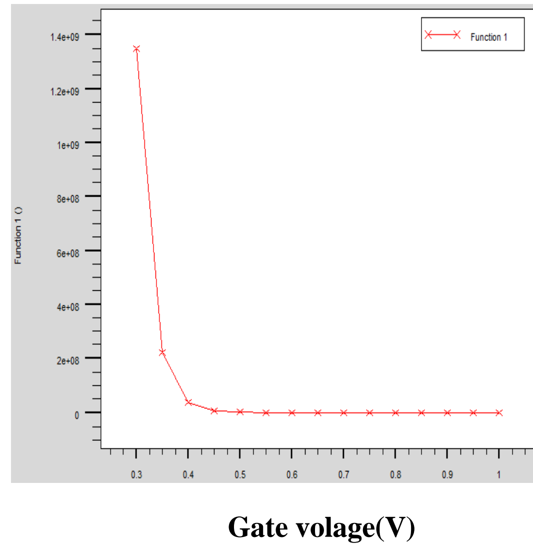
Figure.8: I-D curve with corner effects **Figure.9: I-D curve without corner effects**

The I-D current should increase linearly beyond the threshold voltage of the device with respect to the input gate voltage.these corner effects can be reduced by doping heavily at the corners of the channel.

Gate voltage versus resistance:

Figure.10 shows the graph between input gate voltage and resistance with and without the corner effects.





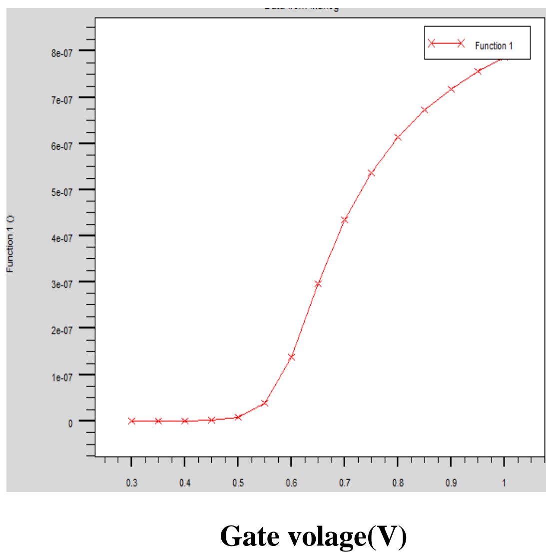
Gate volage(V) **Gate volage(V)**

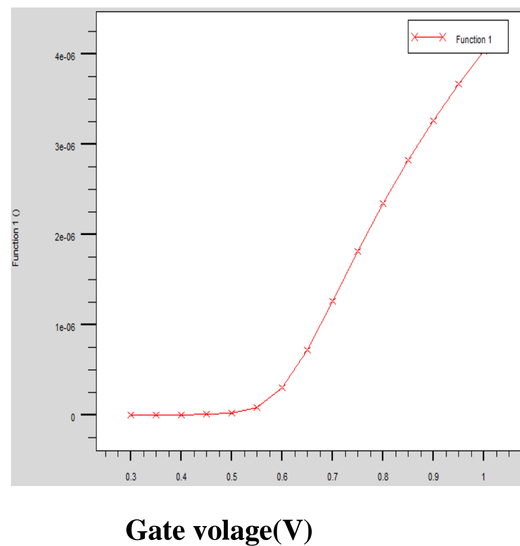
Figure.10: resistance curve with corner effects **Figure.11: resistance curve with corner effects**

The resistance value of the device should decrease linearly and becomes zero when the gate voltage had reached the threshold voltage value.Here in the below graph, the peak value of the resistance i.e the resistance of the device without corner effects is greatly reduced when compared to the resistance with corner effects.

Gate voltage versus transconductance:

The graphs shows relation between input gate voltage and transconductance with and without the reduction of corner effects.





Gate volage(V) **Gate volage(V)**

Figure.12: Transconductance curve with corner effects **Figure.13:Transconductance curve with corner effects**

The transconductance value of the device should increase linearly beyond the threshold value and reached its maximum value.For a good FinFET device the transconductance value should be more.thus, comparing the graphs of the transconductance without and with corner effects,the transconductance value after reducing the corner effects is greatly increased.

Table III constrains for reduction of corner effects

Gate Work Function	4.85
Constant doping value	1e18
Analytical doping value	3e20

Conclusion

The corner effects which degrade the performance of the FinFETs are removed by employing suitable techniques and improvement is observed .A mixed mode LNA circuit and its geometrical parameters are to be varied to obtain optimal Noise Figure and gain,which is the major block in RF transmitter circuit. A FinFET-based cascode narrow band LNA was simulated in TCAD. Six geometrical parameters (Lg, Lun, Wfin, Tox, SW and SL) have been varied over a range from the nominal values and their effect on LNA parameters, Re{Zin}, Im{Zin}, gain and NF, has to be studied.

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